

What is claimed is:

- 1 1. A transistor device comprising:
 - 2 a semiconductor region having a top surface;
 - 3 a source region in the semiconductor region;
 - 4 a drain region in the semiconductor region;
 - 5 a channel region in the semiconductor region between the source region and the
 - 6 drain region;
 - 7 an impurity region within the channel region and spaced from the top surface, the
 - 8 impurity region laterally spaced from the source and drain regions;
 - 9 a gate overlying the channel region; and
 - 10 a gate dielectric between the gate and the channel region.
- 1 2. The device of claim 1 wherein the semiconductor region comprises a region of
2 monocrystalline silicon.
- 1 3. The device of claim 2 wherein the semiconductor region comprises a silicon
2 substrate.
- 1 4. The device of claim 1 wherein the source and drain regions extend into the
2 semiconductor region a first distance, and wherein the impurity region is spaced from the
3 top surface by a distance less than the first distance.
- 1 5. The device of claim 1 wherein the gate dielectric comprises silicon dioxide.

1 6. The device of claim 1 wherein the impurity region comprises a region of an
2 implanted oxygen bearing species in the channel region.

1 7. The device of claim 1 wherein the channel region comprises a strained channel
2 region.

1 8. The device of claim 1 and further comprising:
2 a first sidewall spacer adjacent a first sidewall of the gate;
3 a second sidewall spacer adjacent a second sidewall of the gate;
4 a lightly doped drain region within the semiconductor region adjacent the drain
5 region, the lightly doped drain region disposed beneath the first sidewall; and
6 a lightly doped source region within the semiconductor region adjacent the source
7 region, the lightly doped source region disposed beneath the second sidewall.

1 9. The device of claim 1 and further comprising a second transistor, the second
2 transistor including:
3 a second source region in the semiconductor region;
4 a second drain region in the semiconductor region;
5 a second channel region in the semiconductor region between the second source
6 region and the second drain region;
7 a second gate overlying the channel region; and
8 a second gate dielectric between the gate and the channel region.

1 10. The device of claim 9 further comprising a second impurity region within the
2 second channel region and spaced from the top surface, the second impurity region
3 laterally spaced from the second source region and the second drain region.

1 11. The device of claim 9 wherein the second transistor does not include an impurity
2 region within the second channel region.

1 12. The device of claim 9 wherein the second transistor device comprises an n-
2 channel transistor.

1 13. A method of forming a transistor device, the method comprising:
2 providing a semiconductor region having a top surface;
3 forming source and drain regions in the semiconductor region, the source region
4 being spaced from the drain region by a channel region;
5 forming an oxide region within the channel region and spaced from the top
6 surface; and
7 forming a gate overlying and insulated from the channel region.

1 14. The method of claim 13 wherein the oxide region is formed before forming the
2 source and drain regions.

1 15. The method of claim 13 wherein the oxide region is formed after forming the
2 source and drain regions.

1 16. The method of claim 13 wherein forming an oxide region comprises implanting
2 an oxygen bearing species.

1 17. The method of claim 16 wherein the oxygen bearing species comprises O₂.

1 18. The method of claim 16 wherein forming an oxide region further comprises
2 annealing the transistor device after implanting the oxygen bearing species.

1 19. The method of claim 13 wherein the step of forming source and drain regions
2 includes forming lightly doped source and drain regions.

1 20. The method of claim 13 wherein the step of forming source and drain regions
2 includes forming heavily doped source and drain regions.

1 21. The method of claim 13 wherein forming the gate includes forming a gate
2 dielectric between the gate and the channel region.

1 22. The method of claim 13 wherein the gate dielectric comprises silicon dioxide.

1 23. The method of claim 21 wherein forming the gate includes forming a poly-silicon
2 layer on top of the gate dielectric.

1 24. The method of claim 13 wherein the semiconductor region comprises a silicon
2 substrate.

1 25. The method of claim 13 further comprising:
2 forming a first sidewall spacer adjacent a first sidewall of the gate;
3 forming a second sidewall spacer adjacent a second sidewall of the gate;
4 forming a lightly doped drain region within the semiconductor region adjacent the
5 drain region, the lightly doped drain region disposed beneath the first sidewall; and
6 forming a lightly doped source region within the semiconductor region adjacent
7 the source region, the lightly doped source region disposed beneath the second sidewall.

1 26. A method of manufacturing a CMOS device, the CMOS device including a P-
2 channel MOSFET and an N-channel MOSFET, the method comprising:
3 providing a semiconductor region having a top surface;
4 forming source and drain regions for the P-channel MOSFET in a first part of the
5 semiconductor region, the source region being spaced from the drain region by a P-
6 channel region;
7 forming source and drain regions for the N-channel MOSFET in a second part of
8 the semiconductor region, the source region being spaced from the drain region by an N-
9 channel region;
10 forming at least one oxide region in the semiconductor region spaced from the top
11 surface; and
12 forming a gate for the P-channel MOSFET and a gate for the N-channel
13 MOSFET, the gate for the P-channel MOSFET overlying and insulated from the P-
14 channel region, and the gate for the N-channel MOSFET overlying and insulated from
15 the N-channel region.

1 27. The method of claim 26 wherein forming at least one oxide region includes
2 forming an oxide region between the source and drain regions for the P-channel
3 MOSFET.

1 28. The method of claim 26 wherein forming at least one oxide region includes
2 forming an oxide region between the source and drain regions for the N-channel
3 MOSFET.

1 29. The method of claim 26 wherein forming at least one oxide region includes:
2 forming a first oxide region between the source and drain regions for the P-
3 channel MOSFET; and
4 forming a second oxide region between the source and drain regions for the N-
5 channel MOSFET.